The H25X series single turn encoder is designed for those applications that require 14 or 15 bits of resolution in a compact, easy-to-integrate package. Gray Code and Natural Binary outputs are available for installations using a parallel input with the controller. For simplicity of data transmission, ease of cabling and better noise immunity, an SSI (Serial Synchronous Interface) is also offered. This encoder works with the BEI Serial-to-Parallel converter, allowing for system upgrades from parallel output to SSI.

The H25X is built to the exacting mechanical standards used with the H25 design, including: dual preloaded ABEC 7 bearings; matched thermal coefficients on critical components and electronically centered code disks for high accuracy and stability over a range of environments. Specify the H25X when you need high pointing accuracy and ruggedness in a 14 or 15 bit absolute encoder for your telescope, antenna, robotics, material handling or general industrial automation.

The H25 Absolute Encoder is available with the following certification:

**EN 55011 and EN 61000-6-2**

**UL 13.0071X**

**II 3 G Ex nA IIB T3 Gc**

**Class I, Div. 2, Groups A, B, C & D**
Cable impedance can create a transmission delay, shifting the phase relationship between the clock pulse and the data. If this pulse shift exceeds 180°, then the wrong bit position will be sampled. After the last CLOCK HIGH-to-LOW transition, a minimum of 40 microseconds must pass before the beginning of the next CLOCK series.

Features:
- Synchronous transmission
- Transmission lengths to 1000 feet
- Accepts clock rates from 100 kHz to 1.8 MHz

Data Transmission Sequence:
1. Output driver of the encoder is a MAX 491 transmitter in transmit mode. The recommended receiver is a MAX 491 receiver in receive mode.
2. Controller provides a series of pulses (or differential pulse pairs) on the CLOCK input lines.
3. On the first HIGH-to-LOW CLOCK transition, the encoder latches its data at the current position and prepares to transmit.
4. Controller reads data on the falling edge of the next 15 clock cycles.
5. The first bit is a START bit and is always HIGH.
6. Next comes 13 data bits beginning with the most significant bit (MSB) and ending with the parity bit. On 12 bit encoders, bit 13 is LOW. When parity is not ordered, parity is LOW.
7. After the last CLOCK HIGH-to-LOW transition, a minimum of 40 microseconds must pass before the beginning of the next CLOCK series.

Interfacing Long Data Lines:
Clock impedance can create a transmission delay, in effect, shifting the phase relationship between the clock pulse and the data. If this phase shift exceeds 180°, then the wrong bit position will be sampled by the receiver. As a result, the maximum allowable clock frequency is a function of the cable length. For 24 AWG, stranded, 3 pair cable (BEI part number 37048-003 or equivalent), the group delay is 1.36ns/ft. The table below shows the maximum transmission rate allowable as a function of cable length to ensure a phase shift of less than 90°.

Clock, Maximum (kHz) = 92,000 / Cable Length (ft/CW) for a 90° phase shift.

Max Frequency (kHz) = 1800 900 500 300 200 100

Notes:
1. Mounting is usually done either using the D-style square flange mount, E- or G-style square mounts, or one of the standard face mounts. For example: Consult factory for additional face mount options.
2. The shaft seal is recommended in virtually all installations. The most common exceptions are applications requiring a very low starting torque or those requiring operation at high temperature and high speed.
3. Complementary outputs are recommended for use with line driver type source/sink outputs. When used with differential receivers, this combination provides a high degree of noise immunity.
4. Output ICs: Output ICs are available as either Line Driver LS or NPN Open Collector (OC) types. Line Collectors require pull-up resistors, resulting in higher output source impedance (sink impedance is similar to that of line drivers). In general, use of a Line Driver style output is recommended. Line Drivers source or sink current and their lower impedance mean better noise immunity and faster switching times. Warning: Do not connect any line driver outputs directly to circuit common/0V, which may damage the driver. Unused outputs should be isolated and left floating. Our applications specialists would be pleased to discuss your system requirements and the compatibility of your receiving electronics with Line Driver type outputs.

Parallel Code (14 & 15 Bit):

<table>
<thead>
<tr>
<th>Gray Code</th>
<th>Natural Binary</th>
<th>M14/19 Connector</th>
<th>Cable</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 BIT</td>
<td>15 Bit</td>
<td>14 BIT</td>
<td>15 Bit</td>
</tr>
<tr>
<td>G1</td>
<td>G2</td>
<td>°</td>
<td>°</td>
</tr>
<tr>
<td>G3</td>
<td>G4</td>
<td>°</td>
<td>°</td>
</tr>
<tr>
<td>G5</td>
<td>G6</td>
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<tr>
<td>G7</td>
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<td>°</td>
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<tr>
<td>G9</td>
<td>G10</td>
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</tr>
<tr>
<td>G11</td>
<td>G12</td>
<td>°</td>
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</tr>
<tr>
<td>G13</td>
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<tr>
<td>G15</td>
<td>G16</td>
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<tr>
<td>G17</td>
<td>G18</td>
<td>°</td>
<td>°</td>
</tr>
<tr>
<td>G19</td>
<td>G20</td>
<td>°</td>
<td>°</td>
</tr>
</tbody>
</table>

SLB15 | SLB15 | DIR | DIR | | |
| CASE GROUND | GRN | |

OV (CIRCUIT COMMON) | | |
| BLK | |

+V (SQUARE) | +V (SUPPLY) | +V (VOLTAGE) | +V (VOLTAGE) | +V (VOLTAGE) | |
| LATCH | LATCH | LATCH | U | * |

| RED | RED | |
| SHELD DRAIN | — | BARE |

**SSI Timing**

Direction of Count: Standard is CW increasing when viewed from the shaft end. Pin R is normally HIGH (or N) and is pulled up internally to +V. To reverse the count direction, Pin R must be pulled low (COMMON).

Latch Control: Encoder outputs are active and provide continuous parallel position information when Pin U is HIGH (or N). Pin U is pulled up internally to +V. When Pin U is LOW (COMMON), the encoder outputs are latched to the logic state that is present when the latch is applied and will stay latched until Pin U is no longer grounded.

Driver and Driver Options:

- Parity bit option is available
- Accepts clock rates from 100 KHz to 1.8 MHz
- RS422/485 compatible
- MAX 491 transmitters
- Multi-voltage Line Driver (7272*): 100 mA
- NPN Open Collector (3904*, 7273*). Current sourced by external pull-up resistor
- Limit encoder load to 2.5W
- Supply lines are protected against overvoltage to ±6V
- Open collector outputs with internal pullup resistors. It is recommended to use pullup resistors when using 7272
- Operation at both high temperature and high speed
- CANopen® and NTR
- Gray Code
- Serial Synchronous Interface (SSI)
- SSI Compatible Serial Code (S3):
- Timing Diagram:

**Examples:**
- H25D-SS-12GC-S3-CW-SM18
- H25D-SS-12GC-S3-CW-SM18
- H25D-SS-12GC-S3-CW-SM18

**Notes:**
1. Units Manufactured before April 2007 are LSB Justified
2. Sample Manufactured before April 2007
3. Specials:
4. Higher frequency response may be available. Please consult with the factory.
5. Extended temperature ratings are available in the following ranges: -40 to 70°C, -40 to 85°C, -20 to 105°C and -40 to 105°C depending on the particular model. Extended temperature ranges can affect other performance factors. Please consult with factory for more specific information.
6. NPN Open Collector (OC) types. Open collector outputs with internal pullup resistors. It is recommended to use pullup resistors when using 7272
7. Specials—S at the end of the model number is used to define a variety of non-standard features such as special shaft lengths, voltage options, or special testing. Please consult with the factory for your special requirements.
8. Higher speed output may be available. Please consult with the factory.
9. Consult factory for your specific requirements.
10. Standard pinouts, refer to the facing page.

**Figures**

**Figure 1**
Gray Code

**Figure 2**
Natural Binary